REMARKS

Claims 1-30 remain in the application. Claims 1-30 stand rejected.

Objections to the specification.

The Office Action enumerates several objections to the specification. In the above amendments, Applicants have attempted to adopt the Examiner's suggestions and otherwise remove the objections.

The specification is amended above to include a written description of the subject matter in Figure 16 on page 32. No new matter is introduced because all the statements in the inserted paragraph are found either in the originally filed drawings, or in the Brief Description of the Drawings section of the originally filed specification.

Rejections under 35 U.S.C. §112

The Examiner rejected claims 27-30 under 35 U.S.C. §112, first paragraph as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. The Office Action states that it is not clear how a memory medium can be transferred over a communication interface.

Applicants have amended claims 27-30 above to recite a "method of transferring the computer program . . . comprising the step of transmitting said instructions." As amended, the claims do not require the transmission of a memory medium. Only the instructions are transferred over a communications interface. Since many ways are known in the art to transfer program instructions over a communications interface, Applicants

respectfully submit that one of ordinary skill could make and use the invention of the amended claims 27-30. Applicants respectfully request the Examiner withdraw the rejections of claims 27-30.

The Examiner rejected claims 4-5 and 20 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. The Office Action states that the terms "alive," "refresh," "on less than all" and "user specified policy" are undeterminable.

The "user specified policy" is described in the specification. When "node A requests 150 virtual circuits" and "[o]nly 100 . . . are available through C and node D has only 85 available," then the decision on how to split the routing of the VCB may be "the result of a policy decision (for example, load balancing)" (specification, page 30, lines 4-10). Thus the user specified policy is one, like load balancing, that dictates which virtual circuits of the virtual circuit bunch (VCB) are used.

The "alive" and "refresh" and "less than all" terminology is explained in the specification (page 30, lines 18-24). "In the prior art, there is sometimes a need to send keep alive packets or refresh packets periodically over each virtual circuit to avoid a connection timing out and being broken down. With a virtual circuit bunch, one only needs to send one keep alive packet or refresh packet per virtual circuit bunch and not one for each circuit."

Applicants respectfully submit that these descriptions in the specification are sufficient to distinctly claim the subject matter of the invention using terms "alive," "refresh," "on less than all" and "user specified policy." Accordingly, Applicants

respectfully request the Examiner reconsider and withdraw the rejections of claims 4-5 and 20.

Rejections under 35 U.S.C. §102

The Examiner rejected claims 1, 2, 6, 8 and 18-19 under 35 U.S.C. §102(a) as being anticipated by Dieudonne et al., U.S. Patent 5,793,766 (Dieudonne).

Applicants invention is directed to establishing and using a set of pre-established virtual circuits of a network, such as an asynchronous transfer mode (ATM) network. "[A] group of virtual circuits [is] prestablished in a virtual circuit bunch" (VCB) (specification, page 23, lines 19-20). As described in the specification "a hierarchy of aliases . . . [is] utilized to conveniently refer to portions of . . . a virtual circuit bunch," (specification, page 23, lines 17-20).

Advantages accrue to Applicant's invention because less network traffic is required to use a pre-existing virtual circuit in a VCB according to the invention, than is required to set up, use and break down each virtual circuit as it is needed according to the prior art.

Dieudonne is directed to multiplexing information from a plurality of sources into a stream of asynchronous transfer mode (ATM) cells using "the same logical channel." (Dieudonne, Abstract.)

Applicants respectfully submit that the logical channel of Dieudonne is analogous to the virtual circuit known in the prior art and described in Applicants' specification. Dieudonne does not teach or suggest a group of pre-established logical channels with a common identifier. Therefore a virtual circuit bunch (VCB) is not taught or suggested by

7

Dieudonne. The plurality of input circuits and output circuits shown in FIG. 6 of Dieudonne are analogous to the input and output buffers or registers of the prior art hardware and do not refer to bunches of virtual circuits. The VCB information of Applicants' invention is stored in tables on the controller in Applicants' embodiments, yet the "control unit" of Dieudonne's FIG. 6 is featureless, indicating the conventional control unit which does not have tables recording the VCBs.

Independent apparatus claim 1 recites "a virtual circuit bunch" which is not taught or suggested by Dieudonne for the reasons given above. Therefore a rejection of claim 1 under 35 U.S.C. §102 is improper. Claims 2-9 depend, directly or indirectly, on claim 1, and are allowable for at least the same reason. The Examiner is requested to reconsider the rejections of claims 1, 2, 6 and 8.

Independent method claim 18 recites "a virtual circuit bunch" which is not taught or suggested by Dieudonne for the reasons given above. Therefore a rejection of claim 18 under 35 U.S.C. §102 is improper. Claim 19 depends on claim 18, and is allowable for at least the same reason. The Examiner is requested to reconsider the rejections of claims 18-19.

Claims 10, 21 and 22 were rejected under 35 U.S.C. §102(e) as being anticipated by Suzuki, U.S. Patent 4,884,263.

Suzuki is directed to packet switching in which two or more logical channels are set up in response to a request for a connection. "In the event of an abnormal condition in the first logical channel the message packets are re-routed to the second logical channel." (Suzuki, Abstract.) Suzuki teaches that the multiple logical channels are set up

8

"in response to each call-setup control packet" and "[a]t the end of a call, all the virtual circuits are released by a call-clearing control packet" (Suzuki, column 3, lines 24-32).

Applicants respectfully submit that Suzuki does not teach or suggest that the multiple logical channels be pre-established before an individual call or persist beyond the duration of an individual call, as with a virtual circuit bunch (VCB). In fact, Suzuki teaches the opposite, that the multiple logical channels should be released upon completion of the call. Therefore, Suzuki does not teach or suggest a VCB.

Specifically, computer apparatus claim 10 recites "virtual circuit bunch" which is not taught or suggested by Suzuki for the reasons given above. In addition, claim 10 recites "a single request . . . to establish a plurality of virtual circuits." In contrast, Suzuki teaches that the source terminal must send a plurality of requests, one for each virtual circuit to be established. Specifically, "the number of transmission paths available to the source terminal . . is passed . . . to the source terminal to allow it to send call-setup packets in sequence," (Suzuki, column 5, lines 29-35). Thus the virtual circuit setup of Suzuki is the same as in the prior art. For at least one of these reasons, claim 10 is not anticipated by Suzuki. Applicants respectfully request the Examiner reconsider the rejection of claim 10.

Independent system claim 21 recites "a virtual circuit bunch" which is not taught or suggested by Suzuki for the reasons given above. For at least this reason, the rejection of claim 21 under 35 U.S.C. §102 is improper. Claim 22 depends on claim 21 and is allowable for at least the same reason. Applicants respectfully request the Examiner reconsider the rejections of claim 21-22.

Claims 11-14 and 16 were rejected under 35 U.S.C. §102(b) as being anticipated by Hiller et al., U.S. Patent 5,345,445 (Hiller).

Hiller is directed to allocating data from several telecommunication calls into each cell transmitted over a virtual circuit. Hiller mentions "permanent virtual circuits (PVC)," and "a plurality of . . . PVCs is provisioned", and "only PVCs which have been activated can carry the signals for telecommunications calls" (Hiller, column 2, lines 18-28). However, this does not constitute the virtual circuit bunch (VCB) of Applicants' invention because the network does not treat them as a group.

Hiller does not teach how the PVCs are first set up or eventually broken down, or which processors or switches maintain a list of PVCs and their activity. Hiller only states that the "ingress node signals the egress node . . . the identification of the PVC" (Hiller, column 4, lines 21-27). Thus the PVCs of Hiller are just virtual circuits of the prior art, requested the same way and managed the same way by the network. The PVCs are not handled by the network as a group with a group identifier.

Also, there is only one such group. For example, if all PVCs are full, none are added, and the "system busy" condition occurs (Hiller, column 10, lines 23-26, and Figure 15, item 1216). Because there is only one group, there is no need for names of the group. Thus there is no "hierarchy of aliases . . . utilized to conveniently refer to portions of . . . a virtual circuit bunch," (specification, page 23, lines 17-20).

Only the source terminal knows how many PVCs have been set up and whether they are all busy or not. Only the source terminal applies the methods of FIGs, 15 and 16 of Hiller, cited by the Examiner. The network does not treat the PVCs as a group. Thus a VCB as that term is used in applicants' specification is not taught or suggested by Hiller.

Specifically, claim 11 recites "a virtual circuit bunch" which is not taught or suggested by Hiller for the reasons given above. Also, claim 11 recites "establishing a plurality of virtual circuits . . . in response to a single request." Since Hiller does not disclose how the PVCs are set up, Hiller does not teach or suggest a method other than the prior art method of establishing a plurality of virtual circuits with a corresponding plurality of requests.

Because neither "a single request" nor a "virtual circuit group" is taught or suggested by Hiller, a 102 rejection is improper for claim 11. Claims 12-16 depend on claim 11 and are allowable for at least the same reason. Applicants respectfully request the Examiner reconsider the rejection of claims 11-16.

Apparently, claim 17 is rejected as anticipated by Fisk, U.S. Patent 5,274,643 (page 7 of the Office Action).

Fisk is directed to a network "topology design process" whic accounts for multiple node routing in response to policies that "minimize bandwidth consumption." (Fisk, Abstract.) Virtual circuits are "grouped into virtual paths" in the design process and not during any actual routing. Fisk does not even address actual routing in a network, but only addresses simulations of prior art routing for network design purposes. Applicants respectfully submit that Fisk does not teach or suggest a virtual circuit bunch as that term is used in Applicants' specification.

Independent method claim 17 recites "a virtual circuit bunch" which is not taught or suggested by Fisk for the reasons given above. Because the reference does not teach a significant limitation of Applicants claim, a rejection under 35 U.S.C. §102 is improper. applicants respectfully request the Examiner reconsider the rejection of claim 17.

Rejections under 35 U.S.C. §103

The Examiner rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Hiller.

Claim 3 depends on claim 1 which recites "a virtual circuit bunch" which is not taught or suggested by either Dieudonne or Hiller for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 1 would be improper. Since claim 3 depends on claim 1, the rejection is also improper with respect to claim 3. The Examiner is requested to reconsider the rejection of claim 3.

The Examiner rejected claim 9 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Suzuki.

Claim 9 depends on claim 1 which recites "a virtual circuit bunch" which is not taught or suggested by either Dieudonne or Suzuki for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants' claim, a rejection of claim 1 would be improper. Since claim 9 depends on claim 1, the rejection is also improper with respect to claim 9. The Examiner is requested to reconsider the rejection of claim 9.

The Examiner rejected claim 15 under 35 U.S.C. §103(a) as being unpatentable over Hiller in view of Fisk.

Claim 11 which recites "a virtual circuit bunch" which is not taught or suggested by either Hiller or Fisk for the reasons given above. Claim 11 also recites "a single request" which is not taught or suggested by either Hiller or Fisk for the reasons given above. Because the combination does not teach or suggest every limitation of Applicants'

claim 11, a rejection of claim 11 would be improper. Since claim 15 depends on claim 11, the rejection is also improper with respect to claim 15.

Furthermore, the Examiner does not provide an adequate technical reason or motivation to combine these references. Fisk is directed to designing a network and Hiller packing cells on the network with telephone data. The Hiller network already exists and does not require the design methods of Fisk. Fisk does not profess a need for knowing how telecommunications data are packed into ATM packets, just the number of packets and their destinations. Therefore the Examiner has failed to establish prima facie obviousness, and a rejection under 35 U.S.C. §103 is improper.

Because the combination is improper, and, in any case, does not teach or suggest all the significant limitations of Applicants' claim 15, the rejection is improper. The Examiner is requested to reconsider the rejection of claim 15.

The Examiner rejected claims 23-26 under 35 U.S.C. §103(a) as being unpatentable over Suzuki.

Claims 23-26 each recite "a virtual circuit bunch" which is not taught or suggested by Suzuki for the reasons given above. Therefore, a rejection of claims 23-26 is improper. The Examiner is requested to reconsider the rejection of claim 23-26.

The above amendments are submitted to more particularly describe or claim the Applicants invention and are not made to distinguish over any known reference or prior art. For the reasons given, Applicant submits that the amended claims distinguish over the references cited by the Examiner, and believes that the application is in condition for allowance. The Applicant requests that the Examiner give the application favorable consideration and permit it to issue as a patent.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Should any additional issues remain that might be resolved by an interview or an Examiner's amendment, or if I can be of any assistance in any other way, please do not hesitate to contact me at (202) 756-8682.

Respectfully submitted,

MCDERMOTT, WILL & EMERY
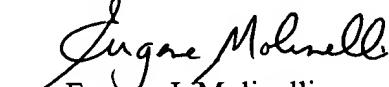
Eugene J. Molinelli
Registration No. 42,901

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 DLS:EJM:pgb
Date: July 14, 1999
Facsimile: (202) 756-8087